IN THE CLAIMS:

7/9/03

Please amend Claims 1, 2, 4, 5, and 6 to read as follows:

1. (Amended) A configurable interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via [an] a first external signal path; and

a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal.

2. (Previously Amended) The configurable interface circuit of Claim 1, further comprising:

an output buffer operative to receive a second [the first] internal signal via a second internal signal path and to provide the second internal signal via the first external signal path.

3. (Original) The configurable interface circuit of Claim 1, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

4. (Amended) The configurable interface circuit of Claim 3, wherein:

the common protocol is a PCI bus protocol.

5. (Amended) The configurable interface circuit of Claim 3, wherein:

the common protocol is an AGP bus protocol.

6. (Amended) The configurable interface circuit of Claim 3, wherein:

the common protocol is an NGP bus protocol.

7. (Original) The configurable interface circuit of Claim 2, further comprising:

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a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal.

8. (Original) The configurable interface circuit of Claim 7, wherein:
the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

9. (Original) The configurable interface circuit of Claim 7, wherein:
the second internal circuit is operable to receive a selected signal that is either the first internal signal or the first external signal from the selector circuit, and inoperable to receive the second internal signal from the selector circuit.

10. (Original) The configurable interface circuit of Claim 7, wherein:
the second internal circuit is operable to provide the second internal signal to the first internal circuit via a fourth internal signal path when the second internal circuit is in a first mode, and to provide the second internal signal to the output buffer via the second internal signal path when the second internal circuit is in a second mode.

11. (Original) The configurable interface circuit of Claim 7, wherein:
the second internal circuit comprises a bus interface.

12. (Original) The configurable interface circuit of Claim 11, wherein:
the second internal circuit is a bus bridge.

13. (Original) The configurable interface circuit of Claim 1, wherein:
the first internal circuit comprises a bus interface.

14. (Original) The configurable interface circuit of Claim 11, wherein:
the first internal circuit is a graphics controller.

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15. (Original) The configurable interface circuit of Claim 2, wherein:

the first internal circuit is operable to receive the second internal signal via the second internal signal path.

16. (Original) The configurable interface circuit of Claim 1, further comprising:

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the first internal circuit via a second internal signal path and to receive the selected signal via a third internal signal path, and

an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

17. (Original) The configurable interface circuit of Claim 16, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

18. (Original) The configurable bus interface circuit of Claim 1, wherein:

the selector circuit is operable to provide a selected signal that is uncorrupted by transmission line effects.

19. (Original) The configurable bus interface circuit of Claim 1, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

20. (Original) The configurable bus interface circuit of Claim 2, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit; and

the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

21. (previously amended) A method for configuring a bus interface circuit comprising:

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A method for configuring a bus interface circuit comprising:

at an internal circuit, receiving a bus bridge signal from an internal bus bridge; and

at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit.

22. (Original) The method of Claim 21, further comprising:

at the external circuit, receiving the bus bridge signal from the internal bus bridge; and

at the external circuit, reflecting the bus bridge signal to the internal I/O circuit.

23. (Original) The method of Claim 21, further comprising:

at the bus bridge, receiving an internal circuit signal from the internal circuit;

at the internal I/O circuit, receiving an external circuit signal from the external circuit;

at the bus bridge, receiving the external circuit signal; and

at the bus bridge, selecting one of the internal circuit signal and the external circuit signal.

24. (Original) The method of Claim 23, wherein:

selecting includes multiplexing.

25. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge is without input buffering.

26. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with a PCI bus.

27. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with a AGP bus.

28. (Original) The method of Claim 21, wherein:

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receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with a NGP bus.

29. (Original) A computer system comprising:

a processing unit coupled to a processor bus;

a memory unit coupled to a memory bus; and

an integrated bus bridge graphics unit, coupled to the memory bus and further operably coupled to provide a signal to an external graphics bus, the integrated bus bridge graphics unit comprising an internal circuit operably configured to avoid signals from the external graphics bus.

30. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further operably coupled to receive a signal from the external graphics bus via an internal I/O circuit.

31. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further configurable to select, and to provide a signal to, one of the internal circuit and the external graphics bus, and is further operably configured to isolate the internal circuit from an external graphics bus signal.

32. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further configurable to select, and to receive a signal from, one of the internal circuit and the external graphics bus.

33. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further operably configured to receive an external signal from the external graphics bus and to isolate the internal circuit from the external signal .

34. (Original) The computer system of Claim 33, wherein:

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the integrated bus bridge graphics unit is further operably configured to receive an external signal via an input buffer from an external circuit, and to isolate the external signal.

35. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is operably configured to provide signals to the internal circuit bufferlessly.

36. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is operably configured to provide signals to the internal circuit uncorrupted by transmission line effects.

37. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with a PCI bus.

38. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with an AGP bus.

39. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with an NGP bus.

40. (Previously Added) A configurable interface circuit comprising:

an internal graphics controller operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via an first external signal path;

a selector circuit coupled to the internal graphics controller via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;

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a bus bridge, comprising a bus interface, operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and

an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

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